WHAT IS CLAIMED IS:

1. A method of receiving code symbols corresponding to an interleaved encoder packet (EP), storing the code symbols separately in first, second and third memories, and inputting the stored code symbols to a turbo decoder in a mobile communication system, the method comprising the steps of:

generating read addresses to read the code symbols according to the size of the EP; and

reading the code symbols at the read addresses from the memories and outputting the read code symbols to the turbo decoder.

2. The method claim 1, where the generating read addresses to read the code symbols comprising steps of;

generating read address of information symbols in the first memory and

generating read address of parity bit symbols in the second and third memory according to the encoder packet size.

3. The method of claim 1, wherein the EP size is one of 408, 792, 1560, 2328, 3096 and 3864 bits.

4. The method of claim 1, wherein the read address generation step comprises the steps of:

generating memory select signals RAM_SEL using a decoder index DEC_IDX identifying a constituent decoder of the turbo decoder and a symbol type signal DT_IDC indicating a code symbol type according to the EP size;

generating temporary read addresses TMP_CS indicating the interleaved positions of the code symbols to be input to the turbo decoder in a subblock to which the code symbols belong; and

generating the read addresses using RAM_SEL, the EP size and the temporary read addresses.

5. The method of claim 1, further comprising the step of generating chip

select signals for the first, second and third memories according to the EP size.

6. The method of claim 1, wherein the chip select signal generation step comprises the steps of:

generating RAM_SEL using DEC_IDX and DT_IDC;

generating TMP_CS; and

generating the chip select signals using RAM_SEL, the EP size and TMP_CS.

7. The method of claim 1, wherein the code symbols are stored at different positions of the first, second and third memories according to the EP size.

8. A data receiving method in a mobile communication system where a transmitter encodes an encoder packet (EP) including information bits and tail bits at a predetermined code rate and subblock-interleaves code symbols of a plurality of encoded subblocks prior to transmission, and a receiver receives the code symbols, stores the code symbols separately in first, second and third memories according to the types of the code symbols, reads the code symbols in a deinterleaving order corresponding to the interleaving, and provides the read code symbols to a turbo decoder having two sequentially operating constituent decoders, the method comprising the steps of:

generating read addresses and chip select signals for the memories using the size of the EP in synchronization to a decoder clock signal; and

outputting code symbols to the two constituent decoders according to the read addresses and the chip select signals.

9. The data receiving method of claim 8, wherein the step of generating the read addresses and the chip select signals comprises the steps of:

setting DT_IDC to 0 when a data symbol corresponding to an information bit is output to the turbo decoder and setting DT_IDC to 1 when a tail symbol corresponding to a tail bit is output to the turbo decoder, each time the decoder clock signal is triggered;

generating a temporary address, TMP_ADDR indicating the interleaved

position of a code symbol to be output to the turbo decoder in a subblock that the code symbol belongs to;

reading the read addresses using TMP_ADDR, the EP size, and RAM_SEL produced by OR-operating DT_IDC and DEC_IDX identifying a constituent decoder; and

generating the chip select signals using RAM_SEL, TMP_ADDR, the EP size, and TMP_CS produced by OR-operating DT_IDC and the inverse of DEC_IDX.

10. The data receiving method of claim 9, wherein when the EP size is one of 408, 792 and 1560, the read addresses RAM0_ADDR, RAM1_ADDR and RAM2_ADDR for the first, second and third memories are determined by

```
if RAM_SEL=0
  RAM0_ADDR=TMP_ADDR
  RAM1_ADDR=2xTMP_ADDR
  RAM2_ADDR=2xTMP_ADDR

else
  RAM0_ADDR=TMP_ADDR
  RAM1_ADDR=2xTMP_ADDR+1
  RAM2_ADDR=2xTMP_ADDR+1
```

11. The data receiving method of claim 10, wherein the chip select signal RAM0_CS for the first memory is TMP_CS and the chip select signals RAM1_CS and RAM2_CS for the second and third memories are 1.

12. The data receiving method of claim 9, wherein when the EP size is 2328, the read addresses RAM0_ADDR, RAM1_ADDR and RAM2_ADDR for the first, second and third memories are determined by

```
if RAM_SEL=0
  RAM0_ADDR=TMP_ADDR
```

RAM1_ADDR=TMP_ADDR
RAM2_ADDR=TMP_ADDR+2328

else
RAM0_ADDR=TMP_ADDR
RAM1_ADDR=TMP_ADDR+2328
RAM2_ADDR=TMP_ADDR

13. The data receiving method of claim 12, wherein the chip select signals RAM0_CS, RAM1_CS and RAM2_CS for the first, second and third memories are determined by

RAM0_CS=TMP_CS
if (RAM_SEL=1) AND (TMP_ADDR 408)
RAM1_CS=0
else
RAM1_CS=1
if (RAM_SEL=0) AND (TMP_ADDR 408)
RAM2_CS=0
else
RAM2_CS=1

14. The data receiving method of claim 9, wherein when the EP size is 3096 or 3864, the read addresses RAM0_ADDR, RAM1_ADDR and RAM2_ADDR for the first, second and third memories are all determined as 1.

15. The data receiving method of claim 14, wherein the chip select signals RAM0_CS, RAM1_CS and RAM2_CS for the first, second and third memories are determined by

RAM0_CS=TMP_CS
if (RAM_SEL=0) AND (TH_OUT=0)

```
 RAM1_CS=1
else
 RAM1_CS=0
if (RAM_SEL=1)  AND (TH_OUT=0)
 RAM2_CS=1
else
 RAM2_CS=0
```

where TH_OUT is 1 if TMP_ADDR is equal to or greater than a predetermined threshold, TH_OUT is 0 if TMP_ADDR is less than the threshold, the threshold is 2352 if the EP size is 3096, and the threshold is 1968 if the EP size is 3864.

16. The data receiving method of claim 8, wherein when the EP size is one of 408, 792 and 1560, or when the EP size is one of 2328, 3096 and 3864 and data symbols are input to the first constituent decoder, three code symbols SYS_DATA, PA0_DATA and PA1_DATA input to the first constituent decoder are determined by

```
if RAM0_CS=1
 SYS_DATA=RAM0_DATA
else
 SYS_DATA=0
if RAM1_CS=1
 PA0_DATA=RAM1_DATA
else
 PA0_DATA=0
if RAM2_CS=1
 PA1_DATA=RAM2_DATA
else
 PA1_DATA=0
```

where RAMx_DATA is a code symbol read at RAMx_ADDR in a (x+1)th memory.

17. The data receiving method of claim 8, wherein when the EP size is one of 2328, 3096 and 3864 and data symbols or tail symbols are input to the second

constituent decoder, or when tail symbols are input to the first constituent decoder, three code symbols SYS_DATA, PA0_DATA and PA1_DATA input to the first or second constituent decoder are determined by

```
if RAM0_CS=1
 SYS_DATA=RAM0_DATA
else
 SYS_DATA=0
if RAM1_CS=1
 PA0_DATA=RAM2_DATA
else
 PA0_DATA=0
if RAM2_CS=1
 PA1_DATA=RAM1_DATA
else
 PA1_DATA=0
```

where RAMx_DATA is a code symbol read at RAMx_ADDR in a (x+1)th memory.

18. An apparatus for receiving code symbols corresponding to an interleaved encoder packet (EP), storing the code symbols separately in first, second and third memories, and inputting the stored code symbols to a turbo decoder in a mobile communication system, the apparatus comprising:

a memory unit having the first, second and third memories, for storing the received code symbols separately as information symbols and parity symbols according to the size of the EP; and

a read address generator for generating read addresses to read the code symbols from the first, second and third memories according to the size of the EP.

19. The apparatus of claim 18, wherein the read address generator comprises:

an input address generator for generating the read addresses of the stored code symbols; and

a chip select signal generator for generating select signals for the first, second and third memories.

20. The apparatus of claim 19, wherein the input address generator comprises:

means for generating the chip select signal RAM_SEL using a decoder index DEC_IDX identifying a constituent decoder of the turbo decoder and a symbol type signal DT_IDC indicating the type of the code symbol to be read according to a EP size;

means for generating a temporary read address TMP ADDR indicating the interleaved position of the code symbol to be read in a subblock to which the code symbol belongs; and

means for generating the read addresses using RAM_SEL, TMP ADDR and the EP size.

21. The apparatus of claim 19, wherein the chip select signal generator comprises:

means for generating RAM_SEL using DEC_IDX and DT_IDC;

means for generating TMP ADDR;

means for generating a temporary chip select signal TMP_CS using DT_IDC and DEC_IDX; and

means for generating the read address using RAM_SEL, TMP_CS, TMP ADDR and the EP size.

22. The apparatus of claim 17, wherein the memory unit further comprises:

a zero inserter for outputting zero symbols according to a chip select signal instead of stored code symbols; and

a switch for switching parity symbols according to the EP size and a chip select signal.

23. The apparatus of claim 21, wherein when the EP size is one of 408, 792 and 1560, the read addresses RAM0_ADDR, RAM1_ADDR and RAM2_ADDR for the first, second and third memories are determined by

```
if RAM_SEL=0
 RAM0_ADDR=TMP_ADDR
 RAM1_ADDR=2xTMP_ADDR
 RAM2_ADDR=2xTMP_ADDR

else
 RAM0_ADDR=TMP_ADDR
 RAM1_ADDR=2xTMP_ADDR+1
 RAM2_ADDR=2xTMP_ADDR+1
```

24. The apparatus of claim 23, wherein the chip select signal RAM0_CS for the first memory is TMP_CS and the chip select signals RAM1_CS and RAM2_CS for the second and third memories are 1.

25. The apparatus of claim 21, wherein when the EP size is 2328, the read addresses RAM0_ADDR, RAM1_ADDR and RAM2_ADDR for the first, second and third memories are determined by

```
if RAM_SEL=0
 RAM0_ADDR=TMP_ADDR
 RAM1_ADDR=TMP_ADDR
 RAM2_ADDR=TMP_ADDR+2328

else
 RAM0_ADDR=TMP_ADDR
 RAM1_ADDR=TMP_ADDR+2328
 RAM2_ADDR=TMP_ADDR
```

26. The apparatus of claim 21, wherein the chip select signals RAM0_CS, RAM1_CS and RAM2_CS for the first, second and third memories are determined by

```
RAM0_CS=TMP_CS
if (RAM_SEL=1) AND (TMP_ADDR  408)
 RAM1_CS=0
else
 RAM1_CS=1
if (RAM_SEL=0)  AND (TMP_ADDR  408)
 RAM2_CS=0
else
 RAM2_CS=1
```

27. The apparatus of claim 21, wherein when the EP size is 3096 or 3864, the read addresses RAM0_ADDR, RAM1_ADDR and RAM2_ADDR for the first, second and third memories are all determined as 1.

28. The apparatus of claim 27, wherein the chip select signals RAM0_CS, RAM1_CS and RAM2_CS for the first, second and third memories are determined by

```
RAM0_CS=TMP_CS
if (RAM_SEL=0)  AND (TH_OUT=0)
 RAM1_CS=1
else
 RAM1_CS=0
if (RAM_SEL=1)  AND (TH_OUT=0)
 RAM2_CS=1
else
 RAM2_CS=0
```

where TH_OUT is 1 if TMP_ADDR is equal to or greater than a predetermined threshold, TH_OUT is 0 if TMP_ADDR is less than the threshold, the threshold is 2352 if the EP size is 3096, and the threshold is 1968 if the EP size is 3864.

29. The apparatus of claim 21, wherein when the EP size is one of 408, 792 and 1560, or when the EP size is one of 2328, 3096 and 3864 and data symbols corresponding to an information bit are input to the first constituent decoder, three code symbols SYS_DATA, PA0_DATA and PA1_DATA input to the first constituent decoder are determined by

```
if RAM0_CS=1
 SYS_DATA=RAM0_DATA
else
 SYS_DATA=0
if RAM1_CS=1
 PA0_DATA=RAM1_DATA
else
 PA0_DATA=0
if RAM2_CS=1
 PA1_DATA=RAM2_DATA
else
 PA1_DATA=0
```

where RAMx_DATA is a code symbol read at RAMx_ADDR in a (x+1)th memory.

30. The apparatus of claim 21, wherein when the EP size is one of 2328, 3096 and 3864 and data symbols or tail symbols are input to the second constituent decoder, or when tail symbols are input to the first constituent decoder, three code symbols SYS_DATA, PA0_DATA and PA1_DATA input to the first or second constituent decoder are determined by

```
if RAM0_CS=1
 SYS_DATA=RAM0_DATA
else
 SYS_DATA=0
if RAM1_CS=1
```

PA0_DATA=RAM2_DATA

else

PA0_DATA=0

if RAM2_CS=1

PA1_DATA=RAM1_DATA

else

PA1_DATA=0

where RAMx_DATA is a code symbol read at RAMx_ADDR in a (x+1)th memory.

31. A data receiving apparatus in a mobile terminal having a turbo decoder, comprising:

an antenna for receiving a radio frequency (RF) signal from a transmitter, the RF signal corresponding to an encoder packet (EP);

a baseband converter for downconverting the RF signal to a baseband signal;

an analog-to-digital converter for converting the baseband signal to a digital signal;

a demodulator for demodulating the digital signal and outputting code symbols;

a memory unit having first, second and third memories, for storing the code symbols separately in the first, second and third memories according to the types of the code symbols and selecting code symbols as a turbo decoder input; and

a memory controller for generating read addresses to read code symbols from the first, second and third memories according to the types of the code symbols.

32. The data receiving apparatus of claim 31, wherein the memory controller comprises:

an read address generator for generating the read address of a code symbol; and

a chip select signal generator for generating a chip select signal to select one of the first, second and third memories.

33. The data receiving apparatus of claim 32, wherein the read address generator comprises:

means for generating the chip select signal RAM_SEL using a decoder index DEC_IDX identifying a constituent decoder of the turbo decoder and a symbol type signal DT_IDC indicating the type of the code symbol to be read according to a EP size;

means for generating a temporary read address TMP ADDR indicating the interleaved position of the code symbol to be read in a subblock to which the code symbol belongs; and

means for generating the read addresses using RAM_SEL, TMP ADDR and the EP size.

34. The data receiving apparatus of claim 32, wherein the chip select signal generator comprises:

means for generating RAM_SEL using DEC_IDX and DT_IDC;

means for generating TMP ADDR;

means for generating a temporary chip select signal TMP_CS using DT_IDC and DEC_IDX; and

means for generating the read address using RAM_SEL, TMP_CS, TMP ADDR and a EP size.

35. The data receiving apparatus of claim 31, wherein the memory unit further comprises:

a zero inserter for outputting a zero symbol instead of the stored code symbol according to the chip select signal; and

a switch for selecting a parity symbol according to a EP size and the chip select signal.

36. The data receiving apparatus of claim 31, wherein the code symbol types are information symbols and parity symbols.

37. A data receiving method in a mobile terminal having a turbo decoder, comprising the steps of:

receiving a radio frequency (RF) signal from a transmitter, the RF signal corresponding to an encoder packet (EP);

down-converting the RF signal to a baseband signal;

converting the baseband signal to a digital signal;

demodulating the digital signal and outputting demodulated code symbols;

storing the code symbols separately in the first, second and third memories according to the types of the code symbols;

generating read addresses to read code symbols as a turbo decoder input from the first, second and third memories according to the type of the code symbols.

38. The data receiving method of claim 37, further comprises the step of generating a chip select signal to select one of the first, second and third memories.

39. The data receiving method of claim 38, wherein the read address generation step comprises the steps of:

generating the chip select signal RAM_SEL using a decoder index DEC_IDX identifying a constituent decoder of the turbo decoder and a symbol type signal DT_IDC indicating the type of the code symbol to be read according to a EP size;

generating a temporary read address TMP ADDR indicating the interleaved position of the code symbol to be read in a subblock to which the code symbol belongs; and

generating the read addresses using RAM_SEL, TMP ADDR and the EP size.

40. The data receiving method of claim 38, wherein the chip select signal generation step comprises the steps of:

generating RAM_SEL using DEC_IDX and DT_IDC;

generating TMP ADDR;

generating a temporary chip select signal TMP_CS using DT_IDC and DEC_IDX; and

generating the read address using RAM_SEL, TMP_CS, TMP ADDR and a EP size.

41. The data receiving method of claim 38, further comprising the steps of:

outputting a zero symbol instead of the stored code symbol according to the chip select signal; and

selecting a parity symbol according to a EP size and the chip select signal.

42. The data receiving method of claim 37, wherein the code symbol types are information symbols and parity symbols.